CLAIMS

What is claimed is:

1. A system comprising:

a communication bus;

a direct memory access (DMA) device coupled to the communication bus, the direct memory access device controlling channels of information, each channel of the channels of information transferring information from a source to a destination in the system via a channel transfer; and

debug control circuitry coupled to the direct memory access device, the debug control circuitry providing debug messages that identify an existence of a DMA channel transfer boundary for at least one predetermined channel.

2. The system of claim 1 wherein the debug control circuitry further comprises:

programmable control means for selecting which of the channels of information controlled by the direct memory access device that the debug messages will identify the existence of channel transfer boundaries.

3. The system of claim 1 wherein one of the debug messages provided by the debug control circuitry indicates that a channel transfer has started for the at least one predetermined channel.

4. The system of claim 3 wherein the one of the debug messages further indicates a status parameter of the at least one predetermined channel.

5. The system of claim 4 wherein the status parameter comprises one of channel priority of the at least one predetermined channel, a utilization factor of the at least one predetermined channel, and whether a transfer error has previously occurred in connection with the at least one predetermined channel.

6. The system of claim 3 wherein the one of the debug messages further indicates a time latency associated with the channel transfer indicating system delay between the direct memory access device receiving a request to begin transferring information and actually transferring the information.

7. The system of claim 1 wherein one of the debug messages provided by the debug control circuitry indicates that a channel transfer has ended for the at least one predetermined channel.

8. The system of claim 1 wherein one of the debug messages provided by the debug control circuitry indicates that each of a plurality of minor loop iterations of the at least one predetermined channel has started.

9. The system of claim 1 wherein one of the debug messages provided by the debug control circuitry indicates that each of a plurality of minor loop iterations of the at least one predetermined channel has ended.

10. The system of claim 1 wherein one of the debug messages provided by the debug control circuitry indicates periodic status of the at least one predetermined channel.

11. The system of claim 1 further comprising:

a plurality of system units, each of the plurality of system units coupled to the communication bus;

wherein the debug control circuitry further comprises a plurality of debug modules for providing the debug messages, each of the plurality of debug modules coupled to a predetermined one of the plurality of system units; and

a debug port logic coupled to the plurality of debug modules for providing the debug messages to a debug port.

12. A system comprising:

a communication bus;

a direct memory access (DMA) device coupled to the communication bus, the direct memory access device controlling channels of information, each channel of the channels of information transferring information from a source to a destination in the system via a channel transfer; and

debug control circuitry coupled to the direct memory access device, the debug control circuitry providing debug messages that periodically provide at least one status parameter for at least one predetermined channel.

13. The system of claim 12 wherein the at least one status parameter further comprises one of channel priority of the at least one predetermined channel, a utilization factor of the at least one predetermined channel, and whether a transfer error has previously occurred in connection with the at least one predetermined channel.

14. The system of claim 12 wherein the debug control circuitry additionally provides debug messages that each indicate that a channel transfer has started.

15. The system of claim 12 wherein the debug control circuitry additionally provides debug messages that each indicate a channel transfer has ended.

16. The system of claim 12 wherein the debug control circuitry is programmable to enable selective generation of the debug messages for each of the channels of information.

17. The system of claim 12 wherein the debug control circuitry further generates a watchpoint indicator that is a predetermined watchpoint condition of the at least one predetermined channel, the predetermined watchpoint condition being a watchpoint condition based upon activity of the direct memory access device.

18. The system of claim 17 wherein the debug control circuitry further generates a plurality of watchpoint indicators, each of which respectively indicating a watchpoint condition of a differing one of the channels of information.

19. The system of claim 12 further comprising:

a control register for storing a control signal that enables and disables the providing of debug messages that periodically provide at least one status parameter for the at least one predetermined channel.

20. The system of claim 12 wherein the direct memory access device implements nested transfers of information within a same channel comprising a plurality of minor loop iterations that form a major loop iteration.

21. The system of claim 12 wherein the debug messages each comprise a multiple bit message having predetermined bit fields comprising a message type field, a channel identification field and a status information field.

22. A system comprising:

a communication bus;

a direct memory access (DMA) device coupled to the communication bus, the direct memory access device controlling multiple channels of information, each channel of the channels of information transferring information from a source to a destination in the system via a channel transfer; and

debug control circuitry coupled to the direct memory access device, the debug control circuitry selectively providing debug messages related to operating parameters of the direct memory access device by being programmable on a per channel basis.

23. The system of claim 22 wherein the operating parameters of the direct memory access device comprise information regarding at least one of whether a transfer boundary occurred and periodic status information.

24. The system of claim 22 wherein the debug control circuitry further provides at least one debug message that includes latency information related to system delay of the direct memory access device starting a channel transfer after a channel transfer request is received by the direct memory access device.

25. A method of real-time debug support in a system comprising:

providing a communication bus;

coupling a direct memory access (DMA) device to the communication bus, the direct memory access device controlling channels of information, each channel of the channels of information transferring information from a source to a destination in the system via a channel transfer;

coupling debug control circuitry to the direct memory access device; and

providing debug messages that identify an existence of a DMA channel transfer boundary for at least one predetermined channel of the channels of information.

26. The method of claim 25 further comprising:

programming and selecting which of the channels of information controlled by the direct memory access device that the debug messages will identify the existence of channel transfer boundaries.

27. The method of claim 25 further comprising:

using one of the debug messages provided by the debug control circuitry to indicate that a channel transfer has started for the at least one predetermined channel.

28. The method of claim 27 further comprising:

using the one of the debug messages to further indicate a status parameter of the at least one predetermined channel.

29. The method of claim 28 further comprising:

using the status parameter to indicate one of channel priority of the at least one predetermined channel, a utilization factor of the at least one predetermined channel, and whether a transfer error has previously occurred in connection with the at least one predetermined channel.

30. The method of claim 27 further comprising:

using the one of the debug messages to further indicate a time latency associated with the channel transfer indicating system delay between the direct memory access device receiving a request to begin transferring information and actually transferring the information.

31. The method of claim 25 further comprising:

using the one of the debug messages provided by the debug control circuitry to indicate that a channel transfer has ended for the at least one predetermined channel.

32. The method of claim 25 further comprising:

using the one of the debug messages provided by the debug control circuitry to indicate that each of a plurality of minor loop iterations of the at least one predetermined channel has started.

33. The method of claim 25 further comprising:

using the one of the debug messages provided by the debug control circuitry to indicate that each of a plurality of minor loop iterations of the at least one predetermined channel has ended.

34. The method of claim 25 further comprising:

using the one of the debug messages provided by the debug control circuitry to periodically indicate a predetermined status parameter of the at least one predetermined channel.

35. The method of claim 25 further comprising:

providing a plurality of system units, each of the plurality of system units coupled to the communication bus;

providing a plurality of debug modules for providing the debug messages, each of the plurality of debug modules being coupled to a predetermined one of the plurality of system units; and

coupling debug port logic to the plurality of debug modules for providing the debug messages to a debug port.

36. A method of real-time debug support in a system comprising:

providing a communication bus;

coupling a direct memory access (DMA) device to the communication bus, the direct memory access device controlling channels of information, each channel of the channels of information transferring information from a source to a destination in the system via a channel transfer; and

coupling debug control circuitry to the direct memory access device for providing debug messages that periodically provide at least one status parameter for at least one predetermined channel.

37. The method of claim 36 further comprising implementing the at least one status parameter as one of channel priority of the at least one predetermined channel, a utilization factor of the at least one predetermined channel, and whether a transfer error has previously occurred in connection with the at least one predetermined channel.

38. The method of claim 36 further comprising additionally providing debug messages that indicate that a channel transfer has started.

39. The method of claim 36 further comprising additionally providing a debug message that indicates a channel transfer has ended.

40. The method of claim 36 further comprising enabling selective generation of the debug messages for each of the channels of information.

41. The method of claim 36 further comprising generating a watchpoint indicator that is a predetermined watchpoint condition of the at least one predetermined channel, the predetermined watchpoint condition being a watchpoint condition based upon activity of the direct memory access device.

42. The method of claim 41 further comprising generating a plurality of watchpoint indicators, each of which respectively indicates a watchpoint condition of a differing one of the channels of information.

43. The method of claim 36 further comprising:

using a control register to store a control signal that enables and disables the providing of debug messages that periodically provides at least one status parameter for the at least one predetermined channel.

44. The method of claim 36 further comprising implementing nested transfers of information within a same channel, each of the nested transfers of information comprising a plurality of minor loop iterations that form a major loop iteration.

45. The method of claim 36 further comprising implementing each of the debug messages as a multiple bit message having predetermined bit fields comprising a message type field, a channel identification field and a status information field.

46. A method of real-time debug support in a system comprising:

providing a communication bus;

coupling a direct memory access (DMA) device to the communication bus, the direct memory access device controlling multiple channels of information, each channel of the channels of information transferring information from a source to a destination in the system via a channel transfer; and

coupling debug control circuitry to the direct memory access device, the debug control circuitry selectively providing debug messages related to operating parameters of the direct memory access device by being programmable on a per channel basis.

47. The method of claim 46 further comprising implementing the operating parameters of the direct memory access device as information regarding at least one of whether a transfer boundary occurred and periodic status information.

48. The method of claim 46 further comprising providing at least one debug message that includes latency information related to system delay of the direct memory access device starting a channel transfer after a channel transfer request is received by the direct memory access device.